PULSE-WIDTH LIMITED CHIP CLOCK DESIGN

ABSTRACT

A method and an apparatus are provided for limiting a pulse width in a chip clock design of a circuit. The circuit receives a clock signal having a clock pulse width. The clock pulse width of the clock signal is detected. It is determined whether the clock pulse width is larger than a maximum clock pulse width. Upon a determination that the clock pulse width is larger than a maximum clock pulse width, the clock pulse width of the clock signal is limited.